An improved locking-time PLL with linearized PFD for reducing Cycle-slipping

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Introduction

- Phase-frequency detections (PFD) plays a crucial role in PLL design to detect the phase difference between reference XTAL input and PLL clock.
- However, the conventional PFD, as shown in Fig. 1(a), suffers from non-linear behavior, as depicted in Fig. 1(b), which causes cycle-slipping phenomenon, resulting in delay the locking state of the PLL.

Circuit Design

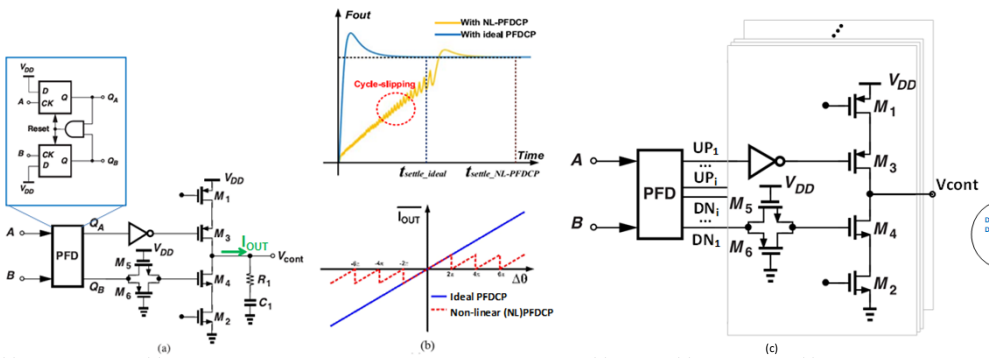


Fig. 1 (a) Conventional PFDCP, (b) relationship between output current I_{out} and cycle-slipping in two cases (1) non-linear (2) linear PFDCP and (c) proposed linearized PFD

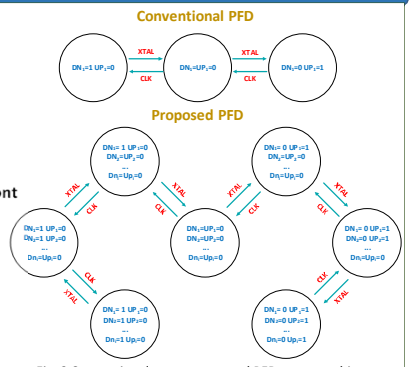


Fig. 2 Conventional versus proposed PFD state-machine

- To improve the PLL locking time, a linearized PFD is proposed in Fig. 1(c) where additional pairs of UP and DN signals are controlled by the state machine illustrated in Fig. 2.
- The following block of PFD, i.e. charge pump (CP) receives the UP and DN signals and generates a linearized I_{out} proportional to the phase difference, overcoming the cycle-slipping issue.

Result

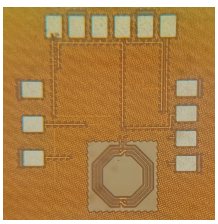
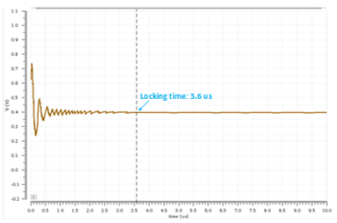
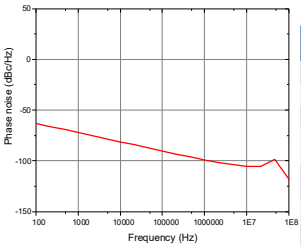


Fig. 3 Chip micro photograph



(a)



(b)

Fig. 4 (a) Locking-time and (b) phase noise of the proposed PLL .

Table I

	Proposed Work	[1] TCASII 2022	[2] TCASII 2022	[4] JSSC 2016
RF (GHz)	3-3.6	2.1-2.6	2-3	2.4
Ref. Freq (MHz)	11	75	50	22.6
Power (mW)	7.1	15.4	4.6	4
Phase Noise (dBc/Hz)	-98.9 @1MHz	-	-92.8 @1MHz	-114 @1MHz
RMS jitter (fs) Integrated ~	718 1k ~ 10 MHz	665 1k ~ 10 MHz	2990 1k ~ 100MHz	970 1k ~ 200MHz
Lock time (μs)	3.6	5.9	0.6	-
Ref. Spur (dBc)	-	-55.4	-53	-65
Tech.	28nm	180nm	40nm	45nm

- The micro-photograph of the proposed PLL is shown in Fig. 3, covering an area of 0.95 mm^2.
- Fig. 4(a) exhibits a locking-time achieving 3.6 us while the phase noise is measured -98.9 dBc at 1 MHz. The proposed PLL performances are shown and compared with other works in Table I.

Conclusion

- The non-ideal behavior of conventional PFD degrades the locking-time specification of PLL.
- To overcome the bottleneck, a linearized PFD is proposed to improve locking-time of PLL while achieving good phase noise with low power consumption.

Acknowledgements

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